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December 12, 2003

Attorney's Docket No. 42P17964

<u>PATENT</u>

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Patent Application of:	
Kumar et al.	Examiner: Not yet assigned
Application No.: Not yet assigned	Art Unit: Not yet assigned
Filed: December 12, 2003	
For: A METHOD AND SYSTEM TO DETERMINE WHETHER A CIRCULAR QUEUE IS EMPTY OR FULL	

Mail Stop Patent Application Commissioner for Patents P.O. Box 1450 Alexandria, Virginia 22313-1450

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Sir:

Enclosed is a copy of Information Disclosure Citation Form PTO-1449 or PTO/SB/08 together with copies of the documents cited on that form. It is respectfully requested that the cited documents be considered and that the enclosed copy of Information Disclosure Citation Form PTO-1449 or PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

Pursuant to 37 C.F.R. § 1.97, the submission of this Information

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Pursuant to 37 C.F.R. § 1.97, this Information Disclosure Statement is being submitted under one of the following (as indicated by an "X" to the left of the appropriate paragraph):

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Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 上のいん

Cory G//Claassen Reg. No. 50, 296

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Substitute for Form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)

Complete if	Known	
Application Number	Not yet assigned	
Filing Date	December 12, 2003	
First Named Inventor:	Kumar et al.	
Art Unit	Not yet assigned	
Examiner Name	Not yet assigned	
Attorney Docket Number	42P17964	

Sheet	1	of	2	Attorney Docket Number	42P17964
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Examiner Initials*	Cite No.1	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant
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		Filing Date	December 12, 2003				
		First Named Inventor:	Kumar et al.				
(use as many sheets as necessary)			ssary)	Art Unit	Not yet assigned		
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	1.			el.com/design/netw sor", October 10, 2	ork/products/npfamily/ixp2800 003.	.htm, "Intel IXP2800	
	2.				Fair Queuing Using Deficit Roulls, 1994, pages 1-26.	ınd Robin", Washington	
	3.		INTEL, "OC-192 DRR Egress Scheduler", Intel IXA Software Building Blocks Developer's Manual, pages 305-317.				
	4.	"Weighted Random Early Detection on the Cisco 12000 Series Router", pages 1-6.					
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